JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results for M.Tech II semester (R16) Regular/Supplementary Examinations Nov-2020

College name: VASIREDDY VENKATADRI INST. OF TECHNOLOGY, NUMBURU, GUNTUR:BQ

Htno	Subcode	Subname	Internal	External	CREDITS
17BQ1D1501	J1501	OPTIMIZATION AND RELIABILITY	32	45	1
17BQ1D1501	J1509	MECHATRONICS ELECTIVE-IV	28	28	1
18BQ1D1501	J2103	FINITE ELEMENT METHODS	37	16	0
18BQ1D5804	J0502	SOFTWARE ENGINEERING ELECTIVE I	34	14	0
18BQ1D8702	J8704	THEORY OF PLATES & SHELLS	31	28	1
18BQ1D8702	J8705	PRESTRESSED CONCRETE ELECTIVEI	30	32	1
18BQ1D8710	J8705	PRESTRESSED CONCRETE ELECTIVEI	27	20	0
18BQ2D6802	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	21	0
18BQ2D6802	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	34	25	1
18BQ2D6802	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	34	19	0
18BQ2D6804	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	45	1
18BQ2D6804	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	40	35	1
18BQ2D6804	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	39	33	1
18BQ2D6804	J6804	DESIGN FOR TESTABILITY	39	29	1
18BQ2D6804	J6805	DSP PROCESSORS AND ARCHITECTURES	39	39	1
18BQ2D6804	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	38	42	1
18BQ2D6804	J6811	EMBEDDED SYSTEM DESIGN LABORATORY	39	40	1
18BQ2D6806	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	39	-1	0
18BQ2D6806	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	33	-1	0
18BQ2D6806	J6803	EMBEDDED REAL TIME OPERATING SYSTEMS EL	33	-1	0
18BQ2D6806	J6804	DESIGN FOR TESTABILITY	36	-1	0
18BQ2D6806	J6805	DSP PROCESSORS AND ARCHITECTURES	35	-1	0
18BQ2D6806	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	35	-1	0
18BQ2D6806	J6811	EMBEDDED SYSTEM DESIGN LABORATORY	32	-1	0

**Note:1)[Last Date to apply for Recounting/Revaluation/Challenge Revaluation is : 20-02-2021]

** Note:**

* -1 in the filed of externals indicates student is absent for the respective subject.

* -2 in the filed of externals indicates student result Withheld for the respective subject.

* -3 in the filed of externals indicates student involved in Malpractice for the respective subject.

Date:11.02.2021

Controller of Examinations